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An Improved Partially Interleaved Transformer Structure for High-voltage High-frequency Multiple-output Applications

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***Abstract*— This paper proposes an improved partially interleaved structure for high-voltage (Several kV) high-frequency (Several hundred kHz) multiple output applications. Six structures are compared with the leakage inductance, AC capacitance and the rate of AC/DC resistance taken into consideration. The proposed structure features lower leakage inductance, smaller AC capacitance and lower rate of AC-DC resistance, which is suitable for high-frequency high-efficiency applications. A planar transformer with the proposed structure was built and tested in an LCLC resonant converter, where the input voltage is 40V, output is 4800V, switching frequency 500 kHz and the efficiency is 96.8%, which validates the analysis.**

Keywords—Planar transformer; Improved partially interleaved structure; high-voltage; high-frequency; multiple-output

I. INTRODUCTION

The high-voltage power supplies with multiple outputs are widely used in Travelling-Wave Tube Amplifiers [1] (TWTAs), lasers [2], Magnetic Resonance Imaging (MRI) [3], where several high-voltage outputs are required by the system. Nowadays, the power supplies are moving toward high power density and high efficiency, especially with the occurrence of novel power switches, such as GaN and SiC devices [4, 5]. In order to achieve high efficiency, resonant topologies are applied to reduce the switching loss. The structure of a high-voltage planar transformer has a crucial role in the performance of a resonant converter since the parasitics are utilized to form a resonant tank [6].

Previous research on planar transformers involved the winding structures [7, 8], the analysis of parasitics [9] and the design of planar transformers [10]. However, most of the researches about planar transformers focused on low-voltage high-current applications, where the high-voltage insulation is not considered. The advantages of planar transformers are very attractive in high-voltage applications.

In this paper, based on the six most promising structures, the winding configurations of high-voltage high-frequency planar transformers are investigated. The details of the six winding configurations are given in Section II. The calculations and comparison of the leakage inductance, the rate of AC/DC resistance and AC capacitance are made in Section III, IV, V, respectively. In Section VI, a planar transformer with the proposed winding configurations was built and tested in LCLC resonant converters.

II. THE WINDING CONFIGURATIONS FOR HIGH-VOLTAGE PLANAR TRANSFORMERS

In high-voltage multiple-output DC-DC converters, as illustrated by Fig. 1, there are always several secondary windings and each secondary winding is connected to a voltage doubler. Every output of a voltage doubler can be used as an output. As a result, there are several outputs.

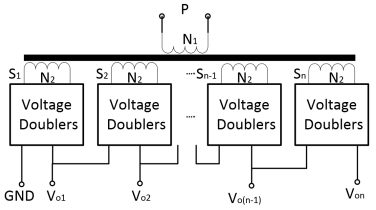
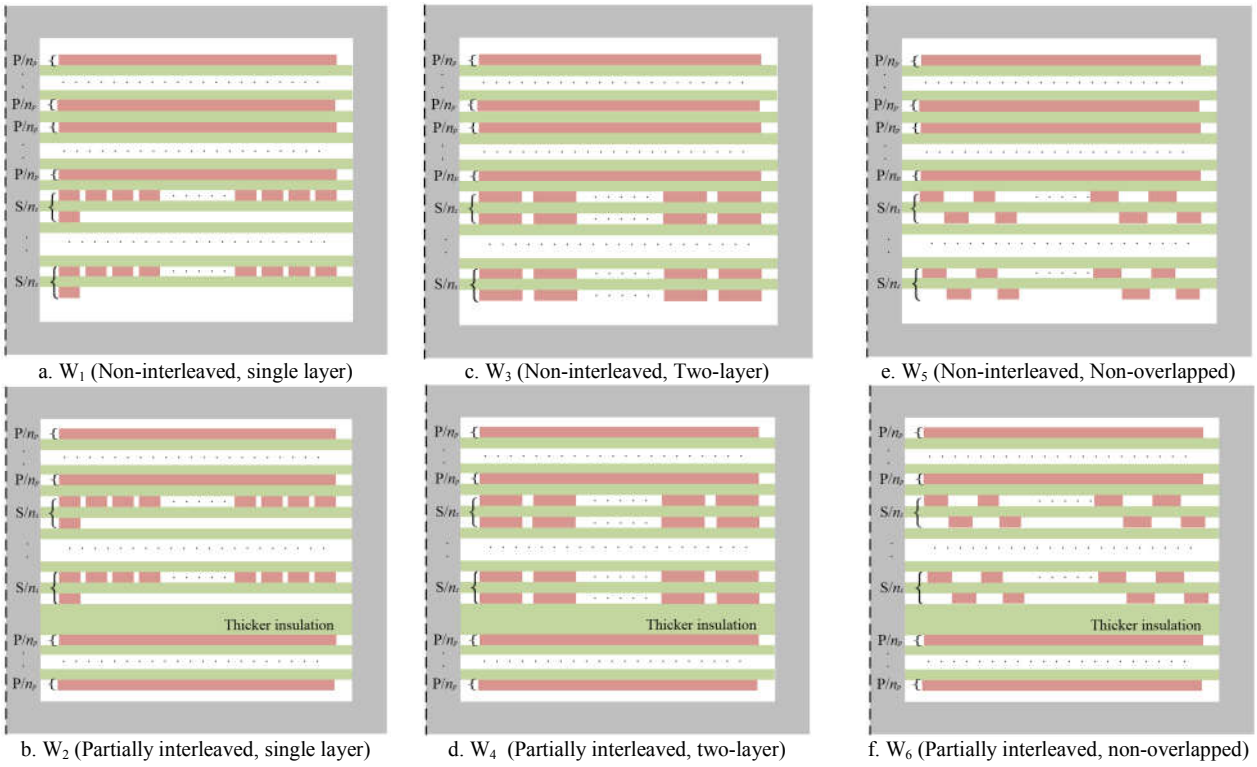


Fig. 1. High-voltage multiple-output transformer with voltage doublers

The six winding configurations are shown in Fig. 2.In Fig. 2(a), Fig. 2(c) and Fig. 2(e), the non-interleaved structures are shown while in Fig. 2(b), Fig. 2(d) and Fig. 2(f), the partially interleaved structures are illustrated. The comparison between the partially interleaved and non-interleaved structures is made to investigate the effect of interleaving on the parasitics.

In a planar transformer, each secondary winding needs at least two layers, with one layer used for the incoming line and the other layer for the outgoing line. The most promising structures are taken into consideration: with single-layer structures shown in Fig. 2(a) and Fig. 2(b), two-layer structures shown in Fig. 2(c) and Fig. 2(d), non-overlapped structures shown in Fig. 2(e) and Fig. 2(f). In order to reduce the leakage inductance, each secondary winding configuration is considered as non-interleaved (Fig. 2(a), Fig. 2(c) and Fig. 2(e)) and partially interleaved (Fig. 2(b), Fig. 2(d) and Fig. 2(f)). In the partially interleaved structure, a thicker insulation is needed to ensure the effectiveness of the insulation.



a. W_1 (Non-interleaved, single layer) c. W_3 (Non-interleaved, Two-layer) e. W_5 (Non-interleaved, Non-overlapped)

b. W_2 (Partially interleaved, single layer) d. W_4 (Partially interleaved, two-layer) f. W_6 (Partially interleaved, non-overlapped)

Fig. 2. Overview of the winding configurations for high-voltage planar transformers

The advantages of the structures shown in Fig. 2 are given as follows. Each secondary winding is distributed in two layers. In the single-layer structure, all the turns in a secondary winding are in the same layer and therefore the intrawinding capacitance is low. In the two-layer structure, half of the turns in a secondary winding are in the upper layer while the other half are in the bottom layer. The space in two layers is fully utilized and minimum DC resistance can be achieved. Similarly, in the non-overlapped structure, half of the turns in a secondary winding are in the upper layer while the other half are in the bottom layer. However, the overlapped area of the secondary winding is minimized to reduce intrawinding capacitance.

The following section will focus on the comparison of the six structures. In order to make a fair comparison, the parameters are given in Table 1 and the magnetic core is FEE 38/16/25. The primary winding has two turns while each secondary winding has twenty turns. Each structure has six secondary windings.

III. COMPARISION OF THE PARASITICS

The main parasitic impedances (leakage inductance, AC/DC resistance and AC capacitance) of the six structures shown in Fig. 2 are compared in this section.

A. Leakage inductance

In high-voltage applications, the leakage inductance is always used as a component in the resonant tank and will affect the resonant condition. As a result, it is important to predict the leakage inductance. The leakage inductance is calculated by the magnetic energy stored in the window

$$E_m = \frac{1}{2}\iiint \mu_0 \mu_r H^2 dV = \frac{1}{2} L_{lk} i_p^2 \tag{1}$$

where μ_r is the relative permeability of the insulation, H is the magnetic field intensity, L_{lk} is the leakage inductance and i_p is the current applied to the primary winding.

As the second layers in the secondary windings of the single layer structure in Fig. 1(a) and Fig. 1(b) are used for

TABLE I. Parameters of high voltage planar transformers

Parameters	Description	Value
w_p	The width of the primary winding	7.27 mm
d_p	The thickness of the primary winding	0.2 mm
d_s	The thickness of the secondary winding	0.07 mm
d_{ni}	The thickness of the normal insulation	0.3 mm
d_{ti}	The thickness of the thicker insulation	1.6 mm
d_{cw}	The safe distance between the windings and the core	1.7 mm

The magnetic core used is FEE 38/16/25 and the material is N87. The widths of the secondary windings in Fig. 1 are 0.27mm, 0.27mm, 0.64mm, 0.64mm, 0.36mm and 0.36mm, respectively.

TABLE II. Equations for leakage inductances

Configurations	Leakage inductance
W_1	$\frac{\mu_0\mu_r MLTn_p^2}{3W_d}[n_p d_p + n_s d_s + \frac{d_{ni}(n_p+1)(2n_p+1)}{2n_p} + \frac{d(n_s-1)(2n_s-1)}{2n_s}]$
W_2	$\frac{\mu_0\mu_r MLTn_p^2}{24W_d}[n_p d_p + n_s d_s + \frac{d_{ni}(n_p+1)(n_p+2)}{n_p} + 3(d_{ti}+d_{ni})]$
W_3, W_5	$\frac{\mu_0\mu_r MLTn_p^2}{24W_d}[4n_p d_p + 8n_s d_s + \frac{2d_{ni}(n_p+1)(n_p+2)}{n_p} + \frac{d_{ni}(2n_s+1)(4n_s+1)}{n_s}]$
W_4, W_6	$\frac{\mu_0\mu_r MLTn_p^2}{24W_d}[n_p d_p + n_s d_s + \frac{d_{ni}(n_p+1)(n_p+2)}{n_p} + 3(d_{ti}-d_{ni})]$

* $d = 2d_{ni} + d_s$

outgoing lines, they do not make contributions to MMF. The magnetic field intensity is calculated by the magneto motive force (MMF). According to [11], the leakage inductance will decrease with the increase of the frequency, but the relative error is acceptable up to several hundred kHz.

The general equations of the leakage inductances of the winding structures are given in TABLE II. With the parameters in TABLE I, the leakage inductances of the winding configurations in Fig. 2 are calculated, which are given in TABLE III.

TABLE III. Calculations results of leakage inductances

Configurations	Leakage inductance (nH)
W_1	125.02
W_2	54.54
W_3, W_5	137.78
W_4, W_6	60.37

Simulations are carried out using Ansys Maxwell and the distributions of the magnetic field at 500 kHz are shown in Fig. 3. Based on the magnetic energy stored in the window, the leakage inductances over different frequencies are calculated and the results are shown in Fig. 4.

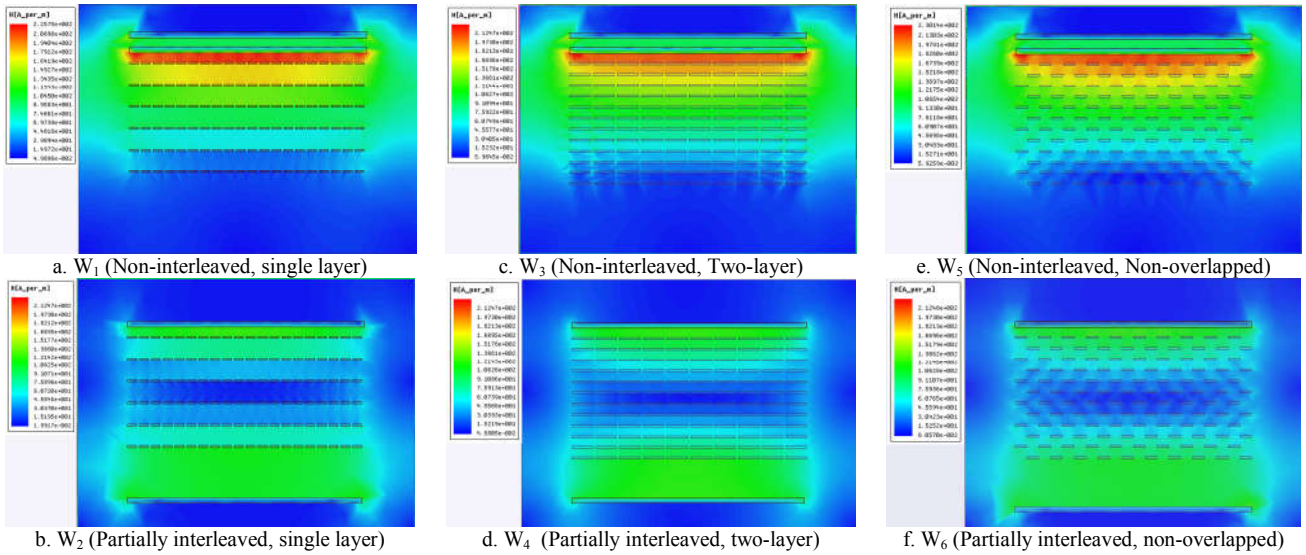
It can be concluded that compared with non-interleaved structures (W_1, W_3 and W_5), the leakage inductances of the partially interleaved structures (W_2, W_4 and W_6) are greatly reduced. Among the partially interleaved structures, the leakage inductances of the single-layer structure are slightly lower than those of W_4 and W_6. It may be explained by the magnetic energy stored among secondary windings are reduced with the single layer structure.

B. AC/DC resistance

AC/DC resistance ratio is an important parameter as it determines the copper loss of the transformer. The AC/DC resistance ratios of different structures shown in Fig. 2 are calculated in Ansys Maxwell and are shown in Fig. 5.

It can be seen from Figure 5 that compared with the non-interleaved structure, the partially interleaved structures (W_2, W_4 and W_6) have lower AC/DC resistance ratio, which means lower copper loss at high frequency. The reasons can be given as follows. In the partially interleaved structures, the magnetic intensity is reduced and as a result, the proximity effect is reduced.

Among three partially interleaved structures (W_2, W_4 and W_6), the single-layer structure (W_2) has the lowest AC/DC resistance ratio. Compared with the other two structures (W_4 and W_6), the magnetic field intensity in the secondary windings is lower, which results in lower proximity effect.



a. W_1 (Non-interleaved, single layer) c. W_3 (Non-interleaved, Two-layer) e. W_5 (Non-interleaved, Non-overlapped)

b. W_2 (Partially interleaved, single layer) d. W_4 (Partially interleaved, two-layer) f. W_6 (Partially interleaved, non-overlapped)

Fig. 3 Distributions of magnetic field @ 500kHz

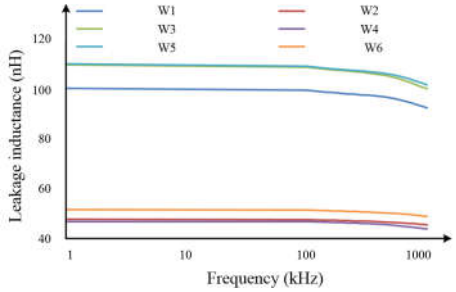


Fig. 4 Leakage inductance simulation results

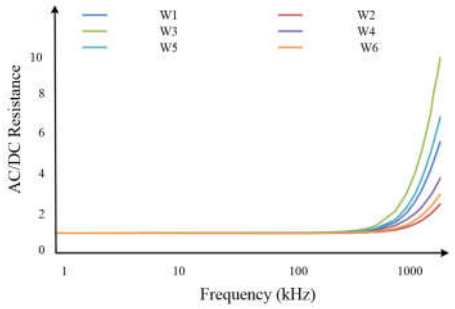


Fig. 5 AC/DC resistance

C. *AC capacitance*

In high-voltage multiple-output DC-DC applications (Fig. 2), as the outputs of the secondary windings are connected to voltage doublers, there are large components of DC voltage in the secondary windings. However, these DC components do not contribute to the resonance conditions because they act only at DC. As a result, the comparison of winding configurations is made in terms of AC capacitance referred to the primary side.

Calculations of AC capacitances are based on the electric energy stored in the core window. With a primary excitation voltage, V_p = 1 V, the voltage on each turn in the secondary windings can be calculated in terms of the primary: secondary turns ratio. The electric energy stored between each pair of winding turns located on different layers can then be calculated as:

$$E_{ci} = \frac{1}{2} C_i V_i^2 \tag{2}$$

where C_i is the capacitance between the turns and V_i is the voltage difference between them. For overlapping turns, C_i can be calculated using the equation for a plane-parallel capacitor. As a result, the total electric energy is given as

$$E_{tot} = \sum E_{ci} \tag{3}$$

and the AC equivalent capacitance referred to the primary side is found as:

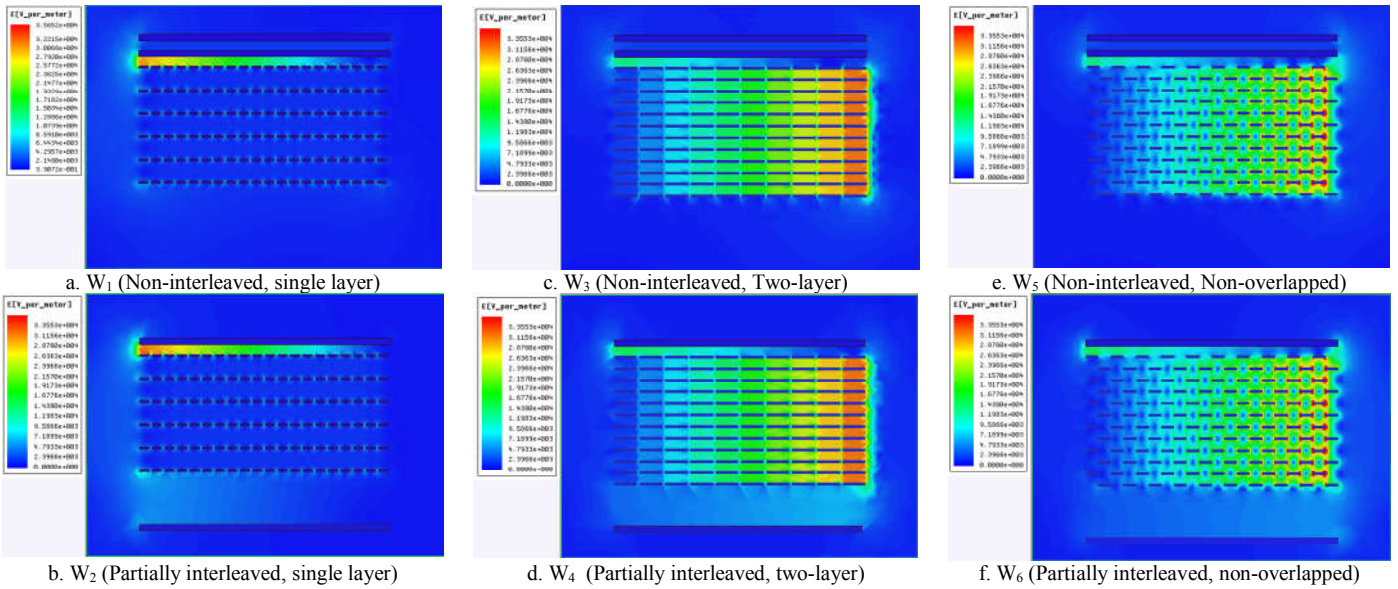
$$C_p = \frac{2\sum E_{ci}}{V_p^2} \tag{4}$$

The calculations of the AC capacitances are based on (4). In addition, simulations of the electric field are carried out in Ansys Maxwell and the resulting distributions of electric field intensity for the different winding configurations are shown in Fig. 6. For ease of comparison, all the color maps in Fig.6 are normalized to the same scale. Both calculation and simulation results are compared in Fig. 7.

It may be seen from Fig. 7 that the AC capacitances of W_3 and W_4 are the largest due to the largest overlapping area of secondary winding turns. Better performance is achieved with windings W_5 and W_6, which are also two-layer structures but with reduced overlapping areas which reduces the electric energy.

It is seen that the AC capacitances of the partially interleaved structures (W_2, W_4 and W_6) are only slightly larger than those of the corresponding non-interleaved structures (W_1, W_3 and W_5). This is due to the large insulation thickness between the primary and secondary windings at the bottom of the core window.

Compared with W_3, W_4, W_5 and W_6, the single-layer



a. W_1 (Non-interleaved, single layer)
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e. W_5 (Non-interleaved, Non-overlapped)
b. W_2 (Partially interleaved, single layer)
d. W_4 (Partially interleaved, two-layer)
f. W_6 (Partially interleaved, non-overlapped)

Fig. 6 Distributions of electric field intensity

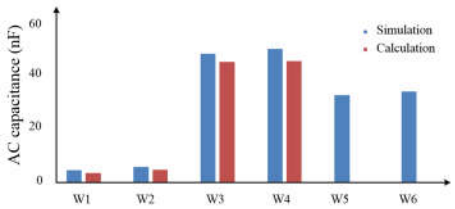

Fig. 7 AC capacitance

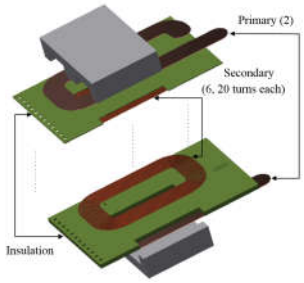

Fig. 8 Planar transformer for the LCLC resonant converter

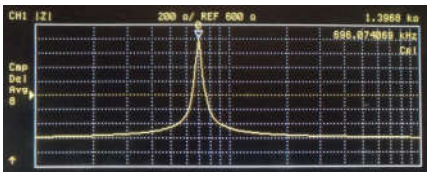

Fig. 9 Measured result in the impedance analyzer

structures have the lowest AC capacitances. As mentioned, the AC capacitance of W_2 is slightly higher than that of W_1. However, it is an acceptable increase.

Based on the above analysis, the partially interleaved, single-layer structure (W_2) achieves the lowest leakage inductance and lowest AC/DC resistance at the cost of a slight increase in AC capacitance (over the lowest capacitance case), which is suitable for high-voltage high-frequency applications.

IV. Experimental Validation

A planar transformer with the partially-interleaved single-layer structure (W_2) was built for a 40V input, 4800V output LCLC resonant converter similar to that shown in Fig. 10. The aim was to use the transformer parasitic impedances to provide Zero-Voltage-Switching (ZVS) and Zero-Current-Switching (ZCS) conditions for all switching components on the primary side.

A. Test of the planar transformer

The shape of the core for the planar transformer is FEE 38/16/25 and the material is TPB 22. The planar transformer (as shown in Fig. 8) has two primary windings and six secondary windings. Each primary winding has one turn. In order to achieve a partially interleaved structure, one primary winding is at the top of the PCB while the other is at the bottom. The six secondary windings are located between the two primary windings and each secondary winding has twenty turns with a single-layer structure. In order to satisfy the requirement of the high-voltage insulation, a thicker insulation(3 mm) is added between the secondary winding and the bottom primary winding.

The planar transformer is tested with a HP 4940 impedance analyzer. The leakage inductance (L_r) is 0.1 μH and the magnetizing inductance (L_m) is 3.4 μH. When all the secondary windings are open circuit, the resonance is between the magnetizing inductance and the parasitic capacitance (C_p). The measured waveform is illustrated in Fig. 9, from which the resonant frequency is found as:

$$f_r = \frac{1}{2\pi\sqrt{L_m C_p}} \tag{5}$$

Therefore, C_p is deduced as:

$$C_p = 13.2nF \tag{6}$$

B. Test of the LCLC resonant converter

The LCLC resonant converter (Fig. 10) with fixed-frequency fixed-duty cycle is widely used in the second stage of a two-stage converter [12, 13]. There are four resonant elements in the resonant tank: series resonant inductance (L_r), series resonant capacitance (C_s), parallel resonant inductance (L_m) and parallel resonant capacitance (C_p). With the transformer leakage inductance as the series resonant inductance, the magnetizing inductance as the parallel resonant inductance and the parasitic capacitance as the parallel resonant capacitance, all the transformer parasitics are incorporated into the resonant tank and only an additional series capacitance is needed.

The LCLC resonant converter with the planar transformer is illustrated in Fig. 11. The input voltage is 40V, the output of each secondary winding is connected to a voltage doubler. The output voltage of each voltage doubler is 800V. The outputs of the six voltage doublers are in series. As a result, each output of a voltage doubler can be used to supply a load with a maximum output voltage of 4800V. The parameters of the LCLC resonant converters are given in TABLE. IV.

Measured waveforms of the LCLC resonant converter with the planar transformer are shown in Fig. 12. It can be seen that the converter switching frequency is 500 kHz. Fig. 12(a) shows the series resonant current $i_r(t)$, the voltage of the

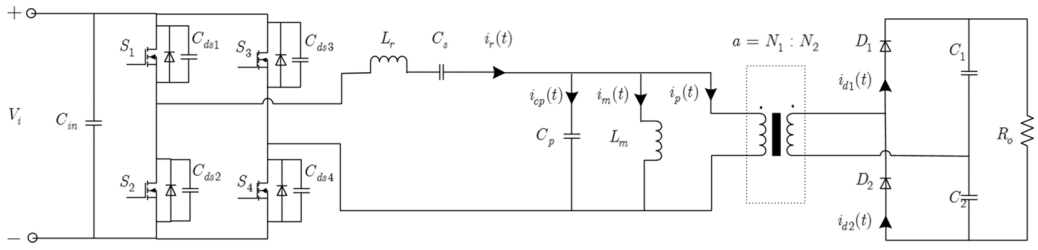

Fig. 10 Planar transformer for LCLC resonant converter

TABLE. IV Parameters of the LCLC resonant converter

Parameter	Value
V_i	40 V
V_o	4800 V
R_o	80 kΩ
L_r	0.1 μH
C_s	1.0 μF
L_m	3.4 μH
C_p	13.2 nF

parasitic capacitor across S_1 (C_{ds1}) and the gate-driver signal of S_1.

It can be seen from Fig. 12(a) that when S_1 is turned on, the voltage of C_{ds1} is zero and the resonant current is also zero, therefore, S_1 operates with Zero-Voltage-Switching (ZVS) and Zero-Current-Switching (ZCS). Therefore the switching loss is minimized.

Fig. 12(b) shows the voltage of the high voltage rectifier diode $v_{d1}(t)$ and the current of the diode $i_{d1}(t)$. It can be seen that when D_1 begins to conduct, both the current and the voltage of the diode are zero. Furthermore, when D_1 is off, both the voltage and current of D_1 are zero. As a result, D_1 operates with ZVS and ZCS.

The analysis of other main switches (S_2, S_3 and S_4) and other high voltage rectifier diodes are similar to S_1 and D_1. With all the main switches and high voltage rectifier diodes achieve ZCS and ZVS, the switching loss is reduced.

When the input voltage is 40V, the input current is 7.35A, the output voltage is 4800V, the output current is 59.88mA, and the load is 80 kΩ, it is calculated that the efficiency is 96.8%.

V. Conclusions

A partially-interleaved transformer with a single-layer winding structure was proposed for high-voltage high-frequency multiple-output application. This structure is compared with other five typical structures. Simulations and calculations show that both the leakage inductance and the AC/DC resistance are lowest with the proposed design. In addition, this structure shares almost the same AC capacitance with the non-interleaved single-layer structure.

A planar transformer with the partially-interleaved single-layer structure was built and tested with the LCLC resonant topology. The switching frequency is 500 kHz while the efficiency was up to 96.8%, which validates that this structure is suitable for high-voltage high-frequency applications.

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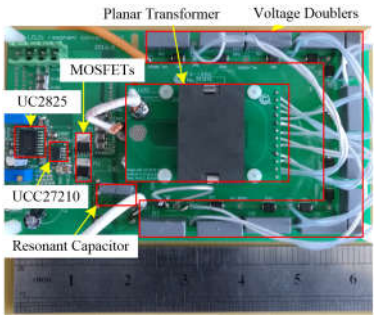
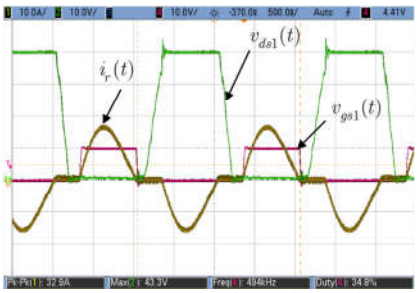
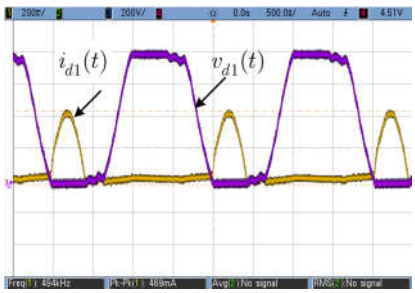


Fig. 11 The LCLC resonant converter



a. Measured waveforms of S_1



b. Measured waveforms of D_1

Fig. 12 Measured waveforms of S_1 and D_1